IN THE DRAWINGS:

The attached sheet of drawings includes changes to Fig. 4. Figure 4 has been amended to include a typographical error. Specifically, the text in Item 420 has been amended from "IDNETIFY" to "IDENTIFY".

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

This is intended as a full and complete response to the Office Action dated June 1, 2006, having a shortened statutory period for response set to expire on September 1, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Status of the Claims

Claims 1-49 are pending in the application. Claims 28-30 and 38-40 have been withdrawn from consideration. Claims 1-27, 31-37, and 41-49 remain pending following entry of this response.

Amendments to the Specification and Drawings

Paragraph [0036] has been amended to correct a minor typographical error. Specifically, the repeated text "the clocks the clock" has been corrected to read "the clock". Figure 4 has also been amended to correct a minor typographical error. Specifically, the text in Item 420 has been amended from "IDNETIFY" to "IDENTIFY". Applicants submit that the amendments to the specification and drawings do not introduce new matter.

Claim Rejections - 35 U.S.C. § 103

Claims 1-7 and 31-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Greene*, U.S. Patent No. 6,775,787 (hereinafter *Greene*) in view of *Gupta et al.,* U.S. Patent No. 5,996,083 (hereinafter *Gupta*), and further in view of *DeLano et al.,* U.S. Patent No. 5,337,415 (hereinafter *DeLano*). Applicants respectfully traverse this rejection.

Brief Statement of the Law of Obviousness

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in

the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the first and third criteria, as described below.

Overview of the Cited References

In the pending rejection, the Examiner cites to *Greene*, *Gupta*, and *DeLano*. *Greene* is directed to power number lookup logic in a processor which determines a power value for a given instruction based on a received instruction type. *Greene,* Col. 4, Lines 35-38. The power values for instructions are provided to an instruction scheduler which schedules instructions for execution such that an abrupt surge in current within a predetermined time is precluded. *Greene,* Col. 4, Lines 43-56. *Gupta* is directed to a power control register that includes a plurality of fields for individually controlling the power consumption of individual functional units within a microprocessor. *Gupta,* Col. 3, Lines 40-44. *DeLano* is directed to a system and method of producing predecode buts from instructions as instructions are copied from a memory system to a cache memory unit. *See DeLano, Abstract.*

Applicant's Response to the Examiner's Argument

With respect to the third criteria of the prima facie case of obviousness, Applicants respectfully submit that the cited references do not teach or suggest all of the claim limitations. Specifically, Applicants submit that the cited references do not teach re-encoding an opcode of an instruction to incorporate a power token. The Examiner states that the claimed subject matter is described in *Greene* at Col. 4, Lines 18-23, Lines 35-50, and Col. 5, Lines 12-21. The cited portions of Col. 4 describe power value lookup logic which uses an instruction type to look up a power value for the instruction. *Greene,* Col. 4, Lines 18-23. The determined power value is transmitted to an instruction scheduler which, as described above, uses the power value to schedule

instruction execution to preclude an abrupt surge in power. *Greene,* Col. 4, Lines 35-56. The power value is also received by dispatch logic. *Greene,* Col. 5, Lines 12-21.

Applicants respectfully submit that the cited sections do no describe re-encoding an opcode of an instruction to incorporate a power token. *Greene* merely states that a power value is obtained from power value lookup logic and transmitted to an instruction scheduler and dispatch logic. The cited sections do not describe re-encoding the opcode of an instruction to incorporate a power token. *Greene,* Col. 4, Lines 18-23, Lines 35-50, and Col. 5, Lines 12-21. Accordingly, Applicants submit that the reference does not teach the claimed subject matter. Applicants respectfully request withdrawal of the rejection.

With respect to the first requirement of the prima facie case of obviousness, Applicants also respectfully submit that there is no suggestion or motivation to combine the reference teachings. With respect to the first requirement, the Examiner states that it would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the method of storing bits indicative of whether functional units within a processor are to be turned off in *Gupta* with the teachings of *Greene*. The Examiner asserts that one of ordinary skill in the art would be motivated to combine *Greene* and *Gupta* in order to increase the power management capabilities and performance of a processor. However, as described below, Applicants respectfully submit that there is no suggestion or motivation to combine the cited references because the combination suggested by the Examiner would render *Gupta* unsatisfactory for its intended purpose. *See* MPEP Sec. 2143.01.

As described above, *Gupta* is directed to a power control register that includes a plurality of fields for individually controlling the power consumption of individual functional units within a microprocessor. *Gupta,* Col. 3, Lines 40-44. *Gupta* criticizes chip-level approaches that dynamically sense instructions in an instruction stream. *See Gupta,* Col. 2, Lines 21-27. *Gupta* criticizes dynamic approaches because they impose a burden on the hardware to monitor and detect the instruction stream. *See* Col. 3, Lines 1-12. *Gupta* states that the hardware has difficulty looking ahead to determine whether certain instructions are going to be issued. *See id. Gupta* instead emphasizes

that a microprocessor which includes the power control register provides *software controllable* power consumption. *See Gupta, Title.* *Gupta* emphasizes that the power control register fields are set by software which has the greater ability to look into the further to determine whether certain functional units will be used to execute an instruction. *Gupta,* Col. 3, Lines 41-63.

Thus, the intended purpose of the power control register in *Gupta* is to provide a mechanism by which *software* can assume control of power consumption within a processor. *See id.* In the pending rejection, the Examiner has suggested that the teachings of *Gupta* should be combined with the teachings of *Greene*. *Greene* describes hardware (an instruction scheduler, power number lookup logic, and power control logic) configured to determine power values for received instructions and schedule the instructions for execution. *Greene,* Col. 4, Lines 18-56. Applicants submit that the combination suggested by the Examiner would render *Gupta* unfit for its intended purpose. Such a combination would render *Gupta* unfit for its intended purpose because the combination would place control of the power control register in *Gupta* with the hardware of *Greene*, thereby removing the emphasized benefit in *Gupta* of controlling power consumption in a processor via software.

If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *See* MPEP § 2143.01 *citing In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Here, as described above, the proposed combination would render the aspects of *Gupta* unfit for their intended purpose. Accordingly, Applicants respectfully submit that there is no suggestion or motivation to combine the cited references. Applicants respectfully request withdrawal of the rejection.

With respect to the first requirement, the Examiner also states that it would have been obvious to one of ordinary skill in the art to combine the teachings of *Delano*, which describes predecoding instructions to determine whether instructions can be executed simultaneously, with the teaching of *Greene* and *Gupta*. The Examiner states that one of skill in the art would be motivated to make the combination in order to

increase the instruction processing speed and achieve faster power management for a processor core.

Applicants respectfully submit that there is not suggestion or motivation to make the asserted combination. Specifically, Applicants respectfully submit that the Examiner does not provide a suggestion or motivation in the references themselves or in the knowledge generally available to one ordinary skill in the art, to combine the reference teachings. *DeLano* merely states that the predecoding can be performed to increase instruction processing speed. *DeLano,* Col. 4, Lines 8-12. *Greene* is directed to instruction scheduling based on power estimation, and *Gupta* is directed to software controllable power consumption. None of the references suggest using predecoding for power estimation or controllable power consumption. Indeed, *DeLano* is merely directed to increasing instruction processing speed, and is not concerned with any affect on power consumption. *DeLano*, Col. 4, Lines 8-12. *DeLano* does not mention the term "power consumption" or "power". Accordingly, Applicants submit that there is no suggestion or motivation to combine the power consumption aspects of *Greene* and *Gupta* with the predecoding aspects of *DeLano*. Accordingly, withdrawal of the rejection is respectfully requested.

Furthermore, to rely on a reference under 35 U.S.C. § 103, the reference must be analogous prior art. *See* MPEP § 2141.01(a). Because *DeLano* is not related to the field of power consumption in processors, Applicants submit that *DeLano* is non-analogous art with respect to *Greene* and *Gupta*. Accordingly, withdrawal of the rejection is respectfully requested.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claims 8, 14 and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Burns et al.*, U.S. Publ. No. 2003/9126479 (hereinafter *Burns*) in view of *DeLano et al.,* U.S. Patent No. 5,337,415 (hereinafter *DeLano*). *Burns* is directed to a digital throttle to monitor the activity of various units of a processor's instruction execution pipeline. *See Burns, Abstract.* If a power state of the processor reaches a threshold, an operating point of the processor is adjusted. *See id.* The Examiner

asserts, as above, that one of skill in the art would be motivated to make the combination of *Burns* and *DeLano* in order to increase the instruction processing speed and achieve faster power management for a processor core.

As described above, Applicants submit that *DeLano* is merely directed to increasing instruction processing speed, and is not concerned with any affect on power consumption. *DeLano*, Col. 4, Lines 8-12. Accordingly, Applicants submit that there is no suggestion or motivation to combine the power consumption aspects of *Burns* and with the predecoding aspects of *DeLano*. Accordingly, withdrawal of the rejection is respectfully requested. Furthermore, because *DeLano* is not related to the field of power consumption in processors, Applicants submit that *DeLano* is non-analogous art with respect to *Burns*. *See* MPEP § 2141.01(a). Accordingly, withdrawal of the rejection is respectfully requested.

Claims 21-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Burns et al.*, U.S. Publ. No. 2003/9126479 in view of *Greene,* U.S. Patent No. 6,775,787, and further in view of *DeLano et al.,* U.S. Patent No. 5,337,415. As described above, Applicants submit that there is no suggestion or motivation to combine the cited references. Applicants further submit that *DeLano* is non-analogous art with respect to the other cited references. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 41 and 45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Greene*, U.S. Patent No. 6,775,787 in view of *DeLano et al.,* U.S. Patent No. 5,337,415. As described above, Applicants submit that there is no suggestion or motivation to combine the predecoding aspects of *DeLano* with the cited aspects of the other references. Applicants further submit that *DeLano* is non-analogous art with respect to the other cited references. Accordingly, Applicants respectfully request withdrawal of the rejection.

Claim 49 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Greene*, U.S. Patent No. 6,775,787 in view of *DeLano et al.,* U.S. Patent No. 5,337,415,

and further in view of *Gupta et al.,* U.S. Patent No. 5,996,083. As described above, Applicants respectfully submit that there is no suggestion or motivation to combine the cited references. Applicants submit that the combination of *Gupta* and *Greene* would render *Gupta* unfit for its intended purpose and furthermore, that there is no suggestion or motivation to combine the predecoding aspects of *DeLano* with the cited references. Also, Applicants submit that *DeLano* is non-analogous art with respect to the other cited references. Accordingly, withdrawal of the rejection is respectfully requested.

Allowable Subject Matter

Claims 9-13, 15-17, 27, 42-44, and 46-48 are objected to as being dependant upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants respectfully acknowledge the allowability of claims 9-13, 15-17, 27, 42-44, and 46-48. However, Applicants submit that the rejection of the base claims has been overcome as described above. Accordingly, withdrawal of the objection and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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Annotated Sheet

ROC920030294US1

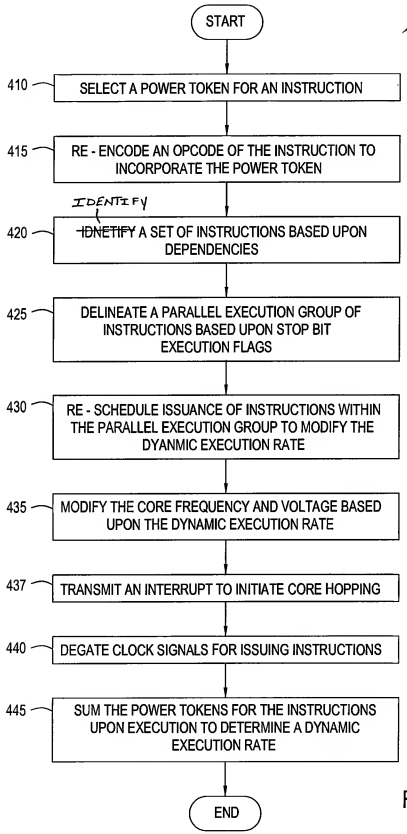

FIG. 4